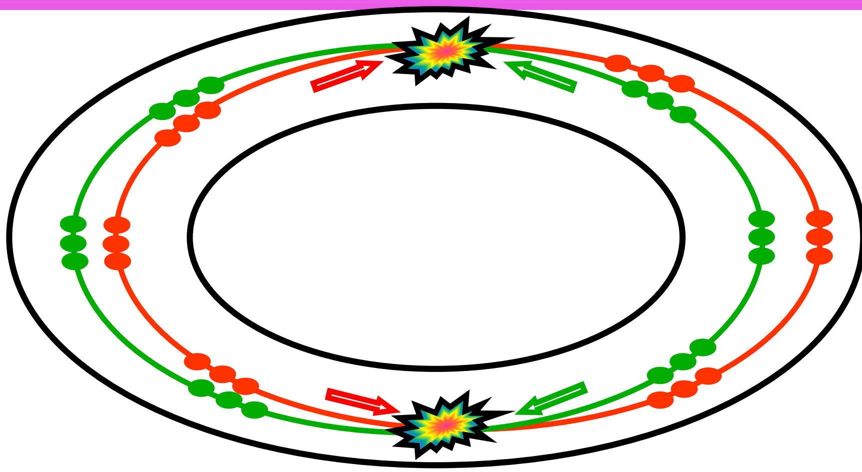
The DØ Level 2 Trigger

James T. Linnemann
Michigan State University
For the DØ L2 Trigger Group
(10 institutions!)

DPF
Aug 12, 2000
Columbus, Ohio

RunII at the Tevatron



Accelerator upgrades will produce >30 times the instantaneous p-pbar beam luminosity of the previous run

Run I (1992-6) Operation		Run II (2000 +) Operation
300 kHz	Detector Input	7.5 MHz
	Trigger Selection	
3 Hz	Data Tape	50 Hz

Trigger Strategy

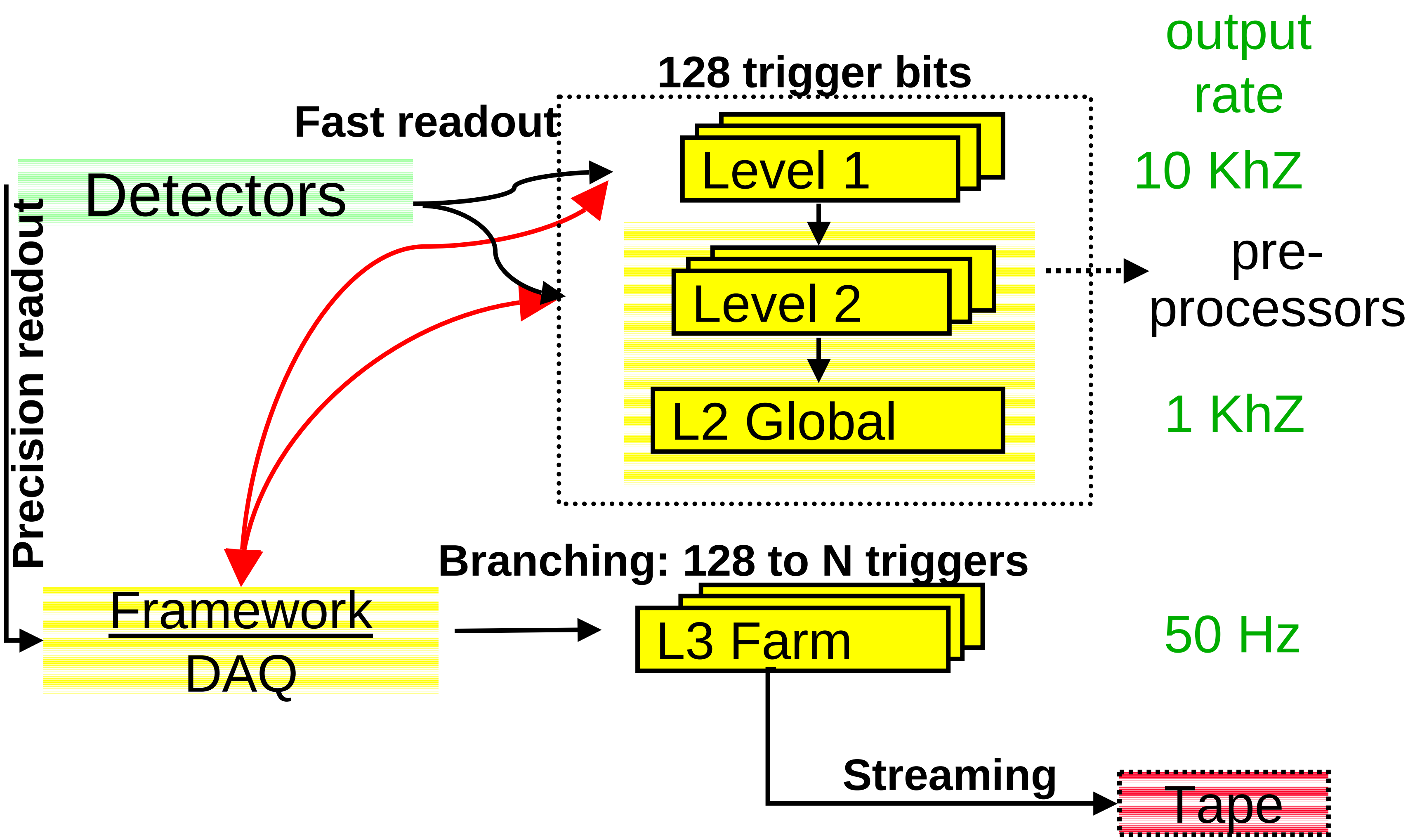
Detectors provide geometric objects
Combined by trigger systems to form
physics objects

	Calor.	Muon	Silicon Vertex	Cent. Tracker	Pre-Shower
e^+,e^-	em clus			track	>> mip
γ	Em clus			no track	>> mip
μ	Mip	μ track		track	
τ	Had clus.			track	
ν	Miss ET				
Jets	Had clus.				
Heavy Flavor	Had clus	μ track	displaced vertex		

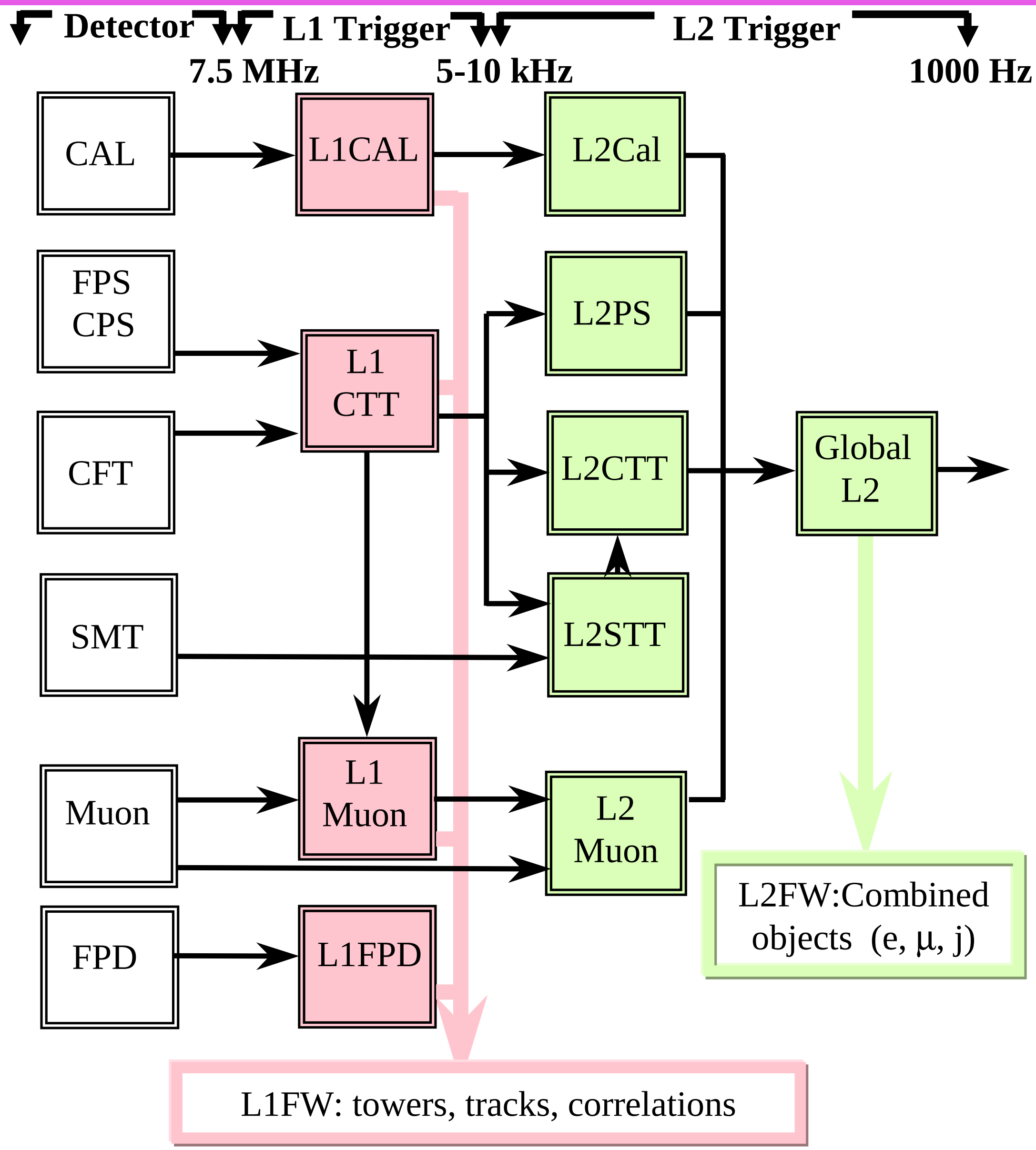
Trigger decisions: count objects
measure object properties
measure object relations

RunII Trigger System

Trigger components and stages



Trigger Organization



Level 2 Requirements

- First event wide trigger decision
- Combine sub-detector information into physics objects (e, jets, μ, missing E_T)
- 10 kHz input rate ⇒ **100 μsec time budget**
- 1 kHz accept rate ⇒ **90% rejection**
- Less than 5% deadtime
- Event order must be maintained!
- 16 front-end buffers for events awaiting decisions
- Hardware support for monitoring and diagnosis
  - And VME readback of all download, status

Stochastic Pipeline

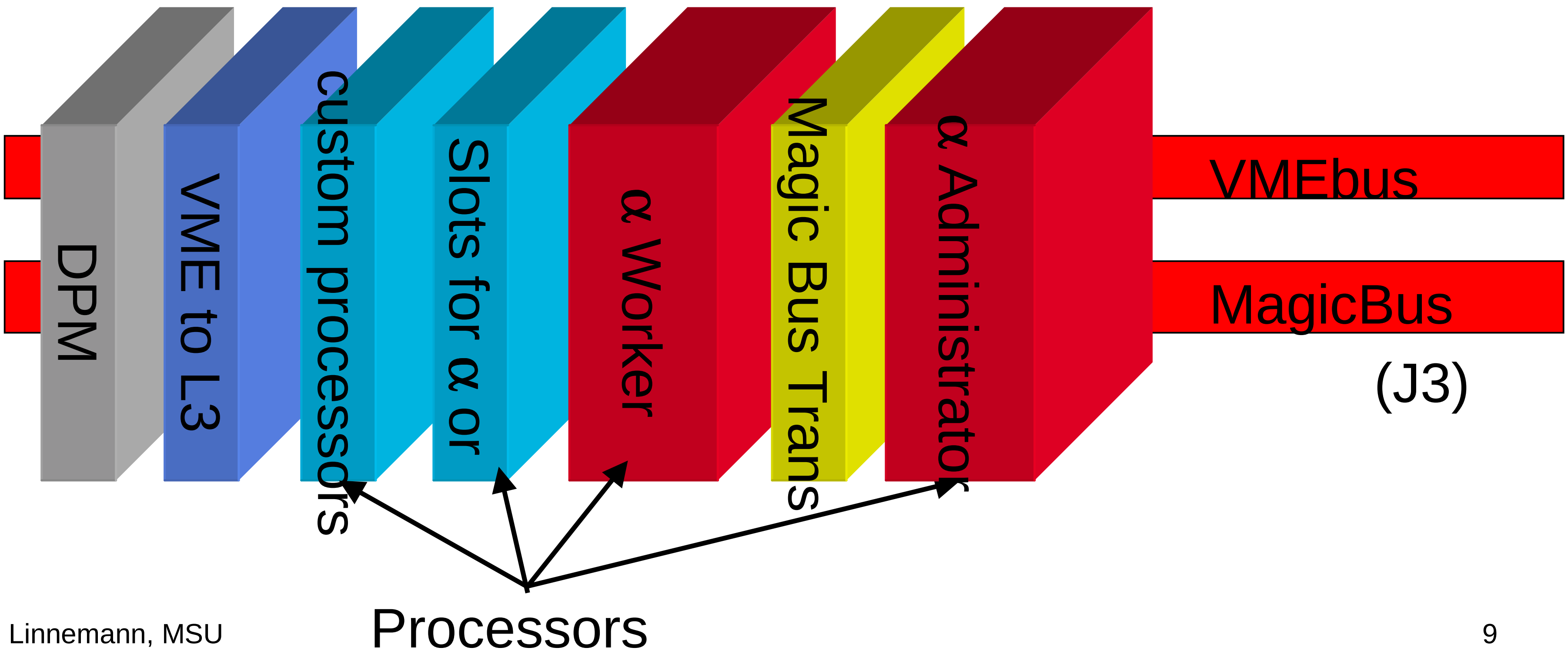
- **2-Stage pipeline: Preprocessor and Global**
  - Preprocessors use detector-specific L1 data
  - Global processor combines detectors
    - Triggers map 1-to-1 with L1 (128 bits)
    - Each trigger programmable (physics objects and cuts)
- **Full set of buffers (16) between stages**
  - Busy raised by front ends not L2
- **Readout driven by hardware framework**
- **Muon, STT have more pipeline stages**
- **Design verified by queueing simulations**

Parallelism

- Preprocessors
  - Muon, tracking, and PS use "geographic parallelism"
  - Calorimeter preprocessor
    - Find EM objects, jets and calculate missing E_T in parallel
    - EM/jet/Missing E_T event synchronous ("lockstep")
    - Can the processing be done in event asynchronous way?
- Global
  - Parallel algorithm?
    - Need a highly parallel algorithm or suffer from Amdahl's law
  - Global farm?
    - Must report answers in same order as arrival

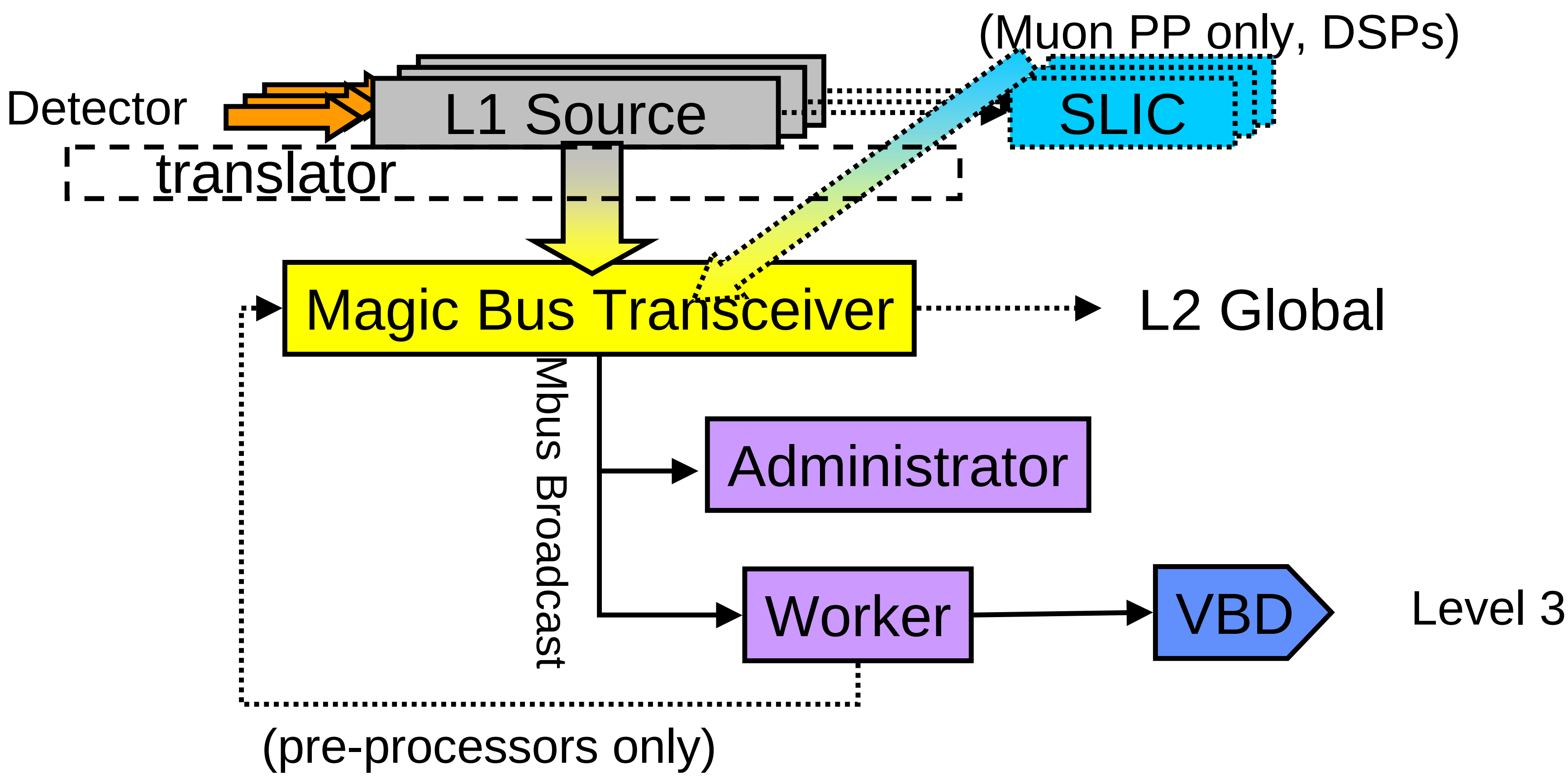
Level 2 Crate (9U VME for Physics)

- Pre-processors and global have similar crates
- Data processing is done by
  - **500 MHz Alpha CPU** cards (=25,000 cycles/event)
  - or processor specific hardware



Data Flow

- In, Out by serial lines: **16MB/s Hotlinks, 106MB/s G-links**
- **MBT** broadcasts to Alphas **320MB/s Magic Bus**



Alpha Processor Card

- **Based on DEC PC164 board**
  - Joint DØ/CDF Project
- **Contains:**
  - **500MHz** 21164 Alpha CPU 2-4 instructions/cycle
  - **128Mb** main memory
  - 267MB/s PCI
    - VME interface
    - 320MB/s MBus interfaces (DMA+PIO) **(all I/O > 1KHz)**
    - Custom Backplane control lines, interrupts
    - Ethernet, EIDE Hard Drive (Linux)
    - 32 channel ECL output port (monitoring)
- **Two functions**
    - administrator controls and manages workers
    - workers process data

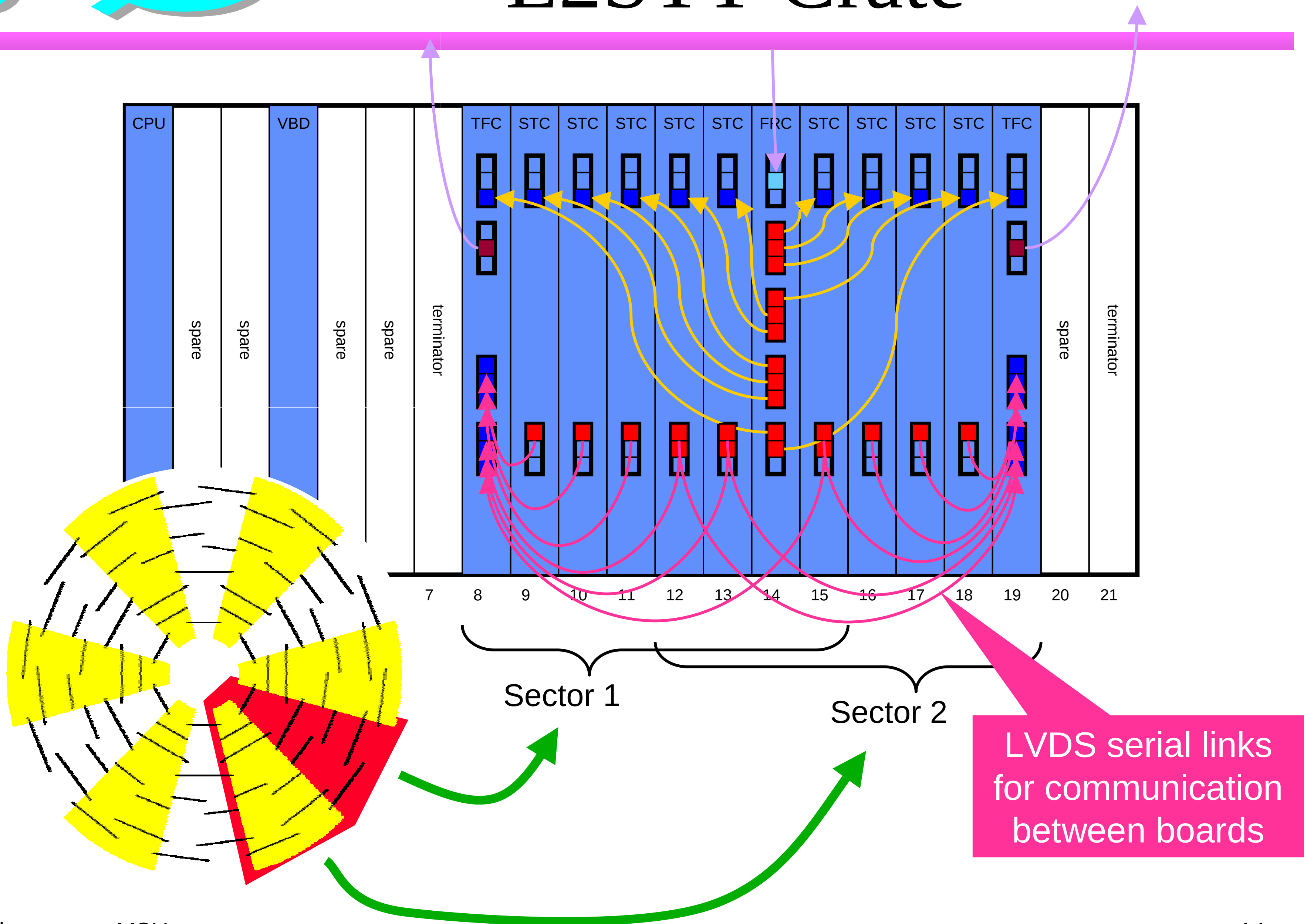
Other Level 2 Cards

- **Magic Bus Transceiver (MBT)** **8 in, 2 out**
  - sends pre-processor outputs to global crate (Hotlinks)
  - broadcasts incoming pre-processor data (Hotlinks) to alphas (MBus)
  - interfaces with Hardware Trigger Framework
- **SLIC (muon system)** **16 in, 2 out**
  - 5 DSPs, 1 master and 4 workers
  - does basic formatting and sorting of data
- **Fiber Input Converter (FIC)**
  - translates G-link to Hotlink for L1 Trigger
- **Serial Fanout (SFO)** **1-6 in, 12 out**
  - fans out **160 MHz Hotlinks** (including test stand data copies)
- **Cable Input Converter (CIC)** **12 in, 12 out**
  - recovers signals for muon processor inputs
- **Bit3 VME-PC controller** **PCI/fiber in, VME/dualport**
  - monitoring and initialization commercial card
- **VME Buffer Driver (VBD)**
  - reads and stores data to send to Level 3 Run I Legacy card

Alpha Environment

- Two environments used:
  - Alpha Linux for most running, debugging
    - modified Linux low level interrupt handler; physical addresses
    - turn off Linux while running--unless crash returns to debugger
    - run test software to debug crate cards in situ
  - bare system still used for some low level testing
- C++ but carefully---
  - No dynamic memory during event loop
  - No RTTI, STL
  - Restricted use of virtual functions
  - Data I/O done for user
    - No user I/O except via error logger during running
  - Run user code unaltered in simulator
    - Relink with simulation version of interfaces

L2STT Crate


CPU
spare
spare
VBD
spare
spare
terminator
TFC
STC
STC
STC
STC
STC
FRC
STC
STC
STC
STC
TFC
spare
terminator
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
Sector 1
Sector 2
LVDS serial links for communication between boards

Motherboard

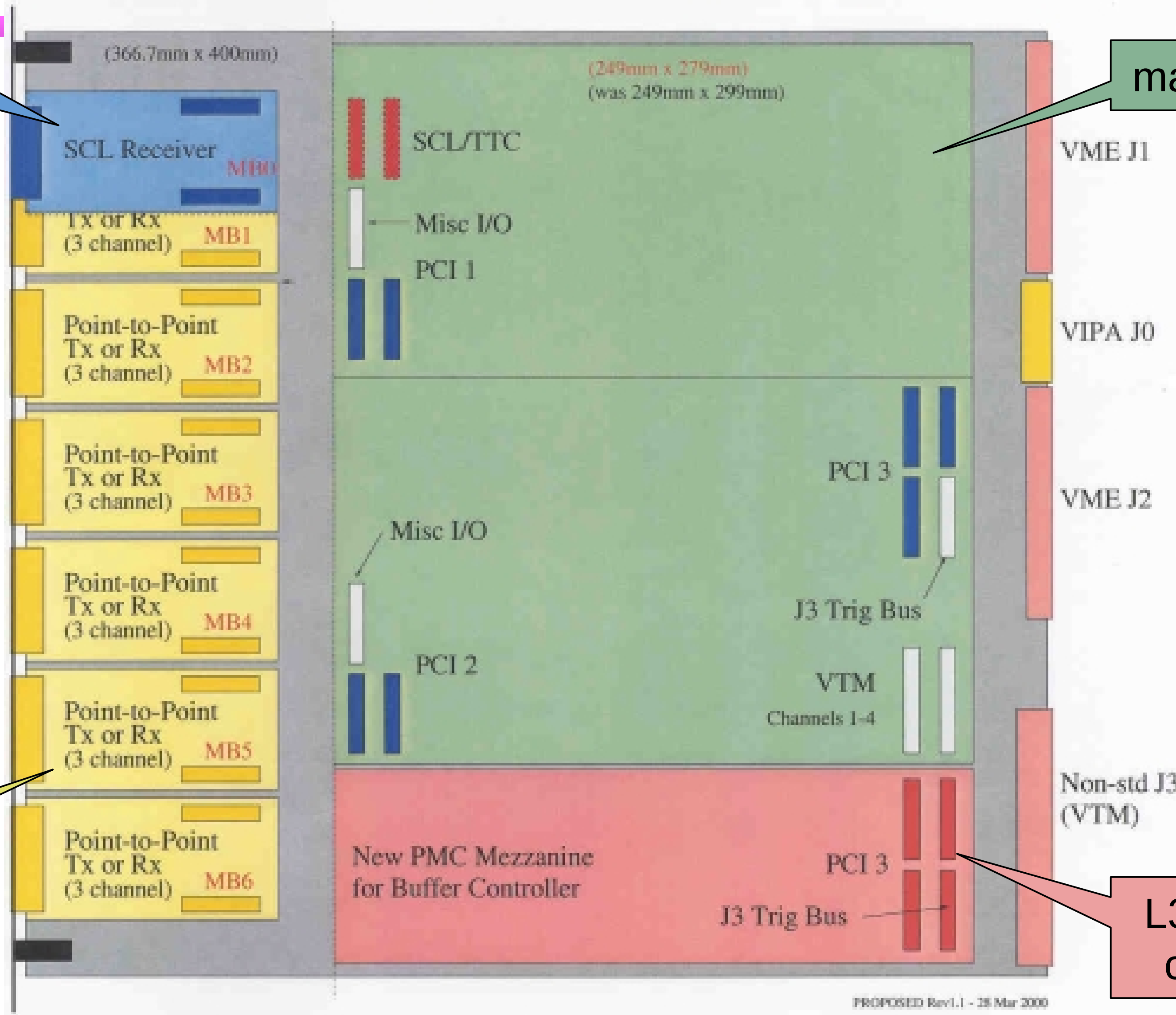
SCL receiver

PCI busses for onboard communication

link tx/rx

main logic

L3 buffer control



STT Card Flavors

- **F**iber **R**oad **C**ard
  - fan out L1 tracker data
  - manage L3 buffers
  - arbitrate VME bus
  - FPGA based
- **S**ilicon **T**rigger **C**ard
  - preprocess Si data
  - associate hits with L1 tracks
  - FPGA based
- **L**VDS **R**x, **T**x cards
  - LVDS to PCI (132MB/s)
  - Input:
    - Event building, buffering
  - Output:
    - fanout
- **T**rack **F**it **C**ard
  - fit trajectory to hits
  - DSP based; C program
- CPU (68K)
  - initialization
  - downloading
  - monitoring
  - Resets
  - VxWorks
- VBD (legacy)
  - L3 readout

Current Status

- **Baseline boards in production (or done)**
- **Online Software (all under release control)**
  - Administrator, worker common code being tested
    - Similar stage with DSP code for SLIC cards
  - Alpha device drivers written, being tuned
  - global script runner and example filters written
  - Most preprocessor algorithms in simulator
- **Installation and commissioning has begun**
  - Vertical slice verification now
  - Test stand running
  - Installing crates and cabling now
  - Baseline system test in fall **2000**

Ready to run in 2001!

STT upgrade 1st year

Queuing Simulations

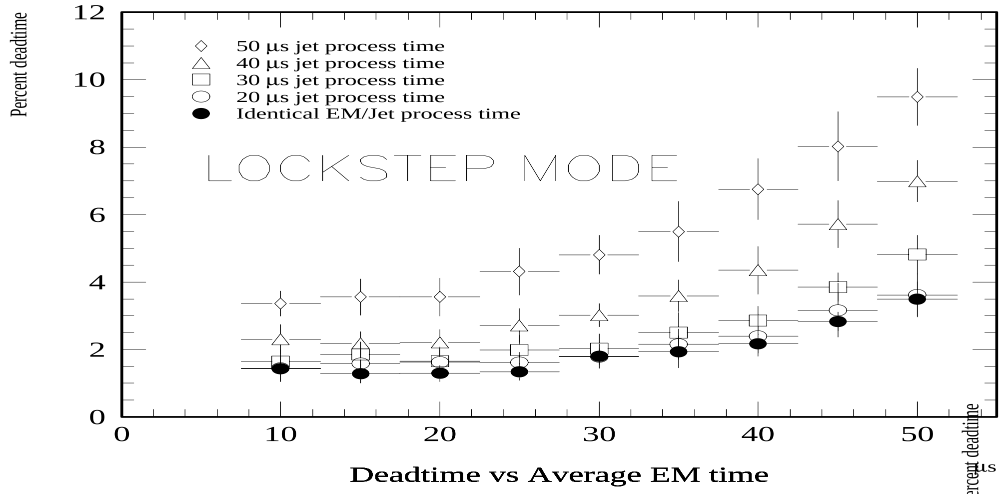
- Use RESQ package from IBM
- Baseline system meets system requirements if:
  - Median Preprocessor time of roughly 50 μsec
  - Median Global time of roughly 50 μsec
  - Avoid long tails in processing time
  - Buffers placed between all elements
- Concerns:
  - Correlation between Cal Workers
  - Retreat paths for Cal and Global

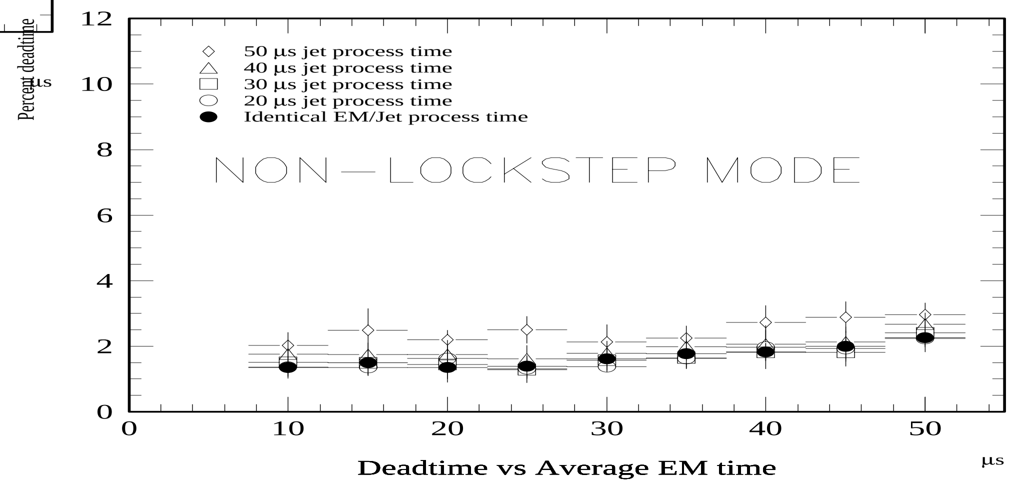
Calorimeter Preprocessor

Missing E_T: (nearly) constant time 45 μsec

EM, jet: vary between 20 and 50 μsec

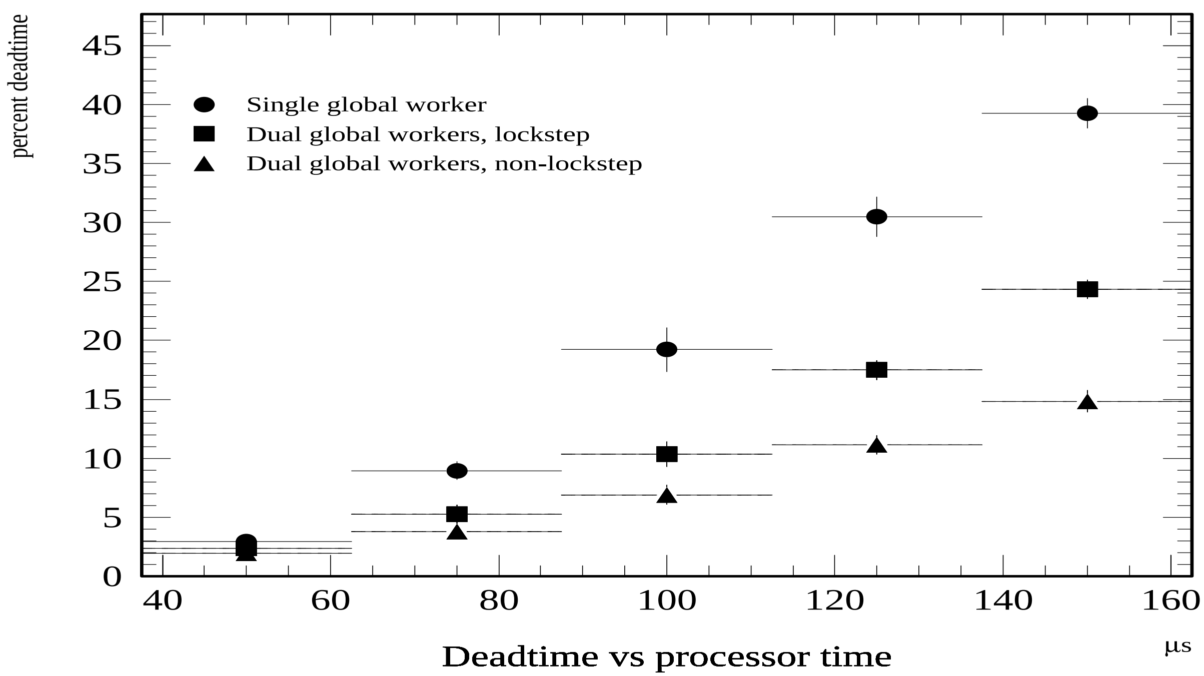
% Deadtime for Event synchronous vs event asynchronous processing





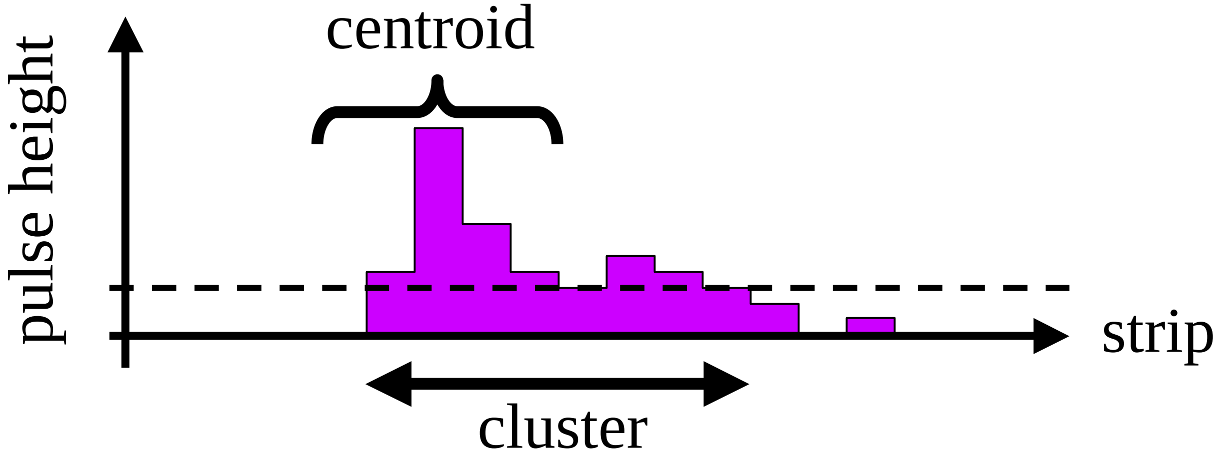
More Global Workers?

- **Parallel algorithm suffers from Amdahl's law**
- **Additional workers**
  - – event synchronous mode (lockstep)
  - – event asynchronous mode (non-lockstep)



Processing of SMT Data

- bad strip mask
  - zero amplitude of flagged strips
- pedestal/gain calibration
  - chip-by-chip lookup table
- clustering algorithm
  - similar to offline, use 5 strips for centroid



Track Fit Algorithm

- require hits in
  - at least 3 of the 4 SMT layers
  - same 30 degree sector
  - at most 2 adjacent barrels
- choose hits
  - closest to trajectory defined by CFT and beam
- linearized χ^2 fit

STT Performance

- generate helical tracks
- intersect with
  - ideal detector geometry
  - nominal assembly tolerance
  - nominal + tent distortions
- reconstruct with ideal detector geometry
- impact parameter resolution includes
  - multiple scattering (50 μm GeV/p_T)
  - beam spot size (30 μm)

Performance

p_T (GeV)	geometry	background pass rate	relative rate	impact par cut (2σ)	relative b efficiency	relative bb eff
		f	$\propto f^3$		ε	$2\varepsilon^3 - (\varepsilon^3)^2$
∞	ideal	4.5%	1	68 μm	1.00	1.00
	nominal	10%	11	86 μm	0.95	0.90
	tent	14%	30	100 μm	0.95	0.88
3.0	ideal	4.5%	1	76 μm	1.00	1.00
	nominal	9%	8	94 μm	0.94	0.88
	tent	12%	19	110 μm	0.94	0.88
1.5	ideal	4.5%	1	96 μm	1.00	1.00
	nominal	7.5%	4.6	108 μm	0.96	0.91
	tent	10%	11	120 μm	0.96	0.91

assume: luminous region =22 cm, three tracks with S>2,
impact parameter of b-tracks =250 μm